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(71) Applicant: LUCENT TECHNOLOGIES INC.
Murray Hill, New Jersey 07974-0636 (US)

(72) Inventors:
• Alers, Glenn B.
Chatham, New Jersey 07928 (US)
• Choi, Seungmoo
Orlando, Florida 32835 (US)
• Merchant, Sailesh Mansinh
Orlando, Florida 32835 (US)
• Roy, Pradip Kimar
Orlando, Florida 32819 (US)

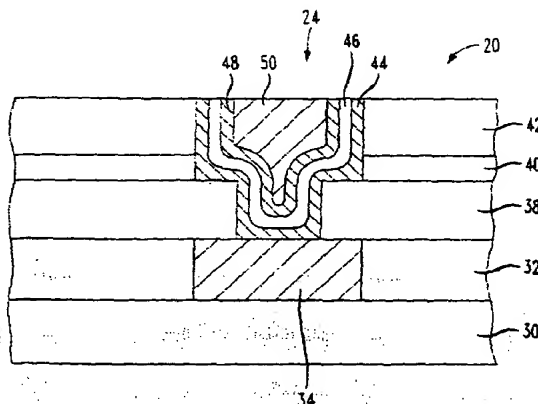
(74) Representative: Williams, David John et al
Page White & Farrer,
54 Doughty Street
London WC1N 2LS (GB)

(54) **Integrated circuit device having dual damascene capacitor and associated method for making**

(57) An integrated circuit device includes a dielectric layer (42) having an opening therein, and a capacitor comprising in stacked relation a lower electrode (44) lining the opening, a capacitor dielectric layer (46) adjacent the lower electrode, and an upper electrode (48,50) adjacent the capacitor dielectric layer. The capacitor has a substantially planar upper surface substantially flush

with adjacent upper surface portions of the dielectric layer. Additionally, the edges of the lower electrode and the capacitor dielectric layer preferably terminate at the upper surface of the capacitor. Also, the capacitor dielectric may include a high-k, high quality and low leakage dielectric, and which prevents the reduction of the capacitor dielectric by the metal of the upper and lower metal electrodes.

FIG. 1



EP 1 022 783 A3



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The present search report has been drawn up for all claims			
Place of search MUNICH		Date of completion of the search 11 April 2001	Examiner Blackley, W
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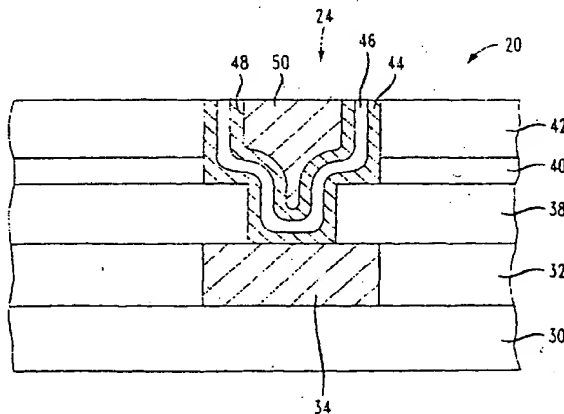
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FIG. 1





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MUNICH		11 April 2001	Blackley, W
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